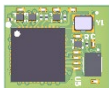
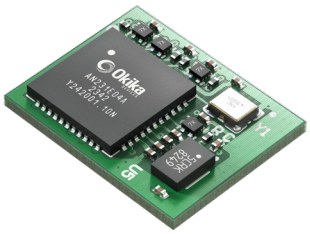
OTC9300L

Chameleon™
Field Programmable
Analog Module



Actual Module Size



Summary

The Chameleon™ module contains an Okika Devices Field Programmable Analog Array (FPAA) with onboard EEPROM and reference oscillator in a tiny 14x11 mm LGA-32 form factor. While other modules in the Chameleon™ family ship pre-programmed as fixed function devices, the OTC9300L is a blank module that can be programmed in system through SPI interface or by using Okika's Chameleon programming board and 3.3V SPI EEPROM programmer. New functions are developed and simulated using Okika's Anadigm Designer 2 software.

Chameleon modules feature Okika's FlexAnalog™ FPAA technology, which leverages switched capacitor analog design and highly flexible routing matrix to implement over 40 configurable analog modules (CAMs) with adjustable parameters. A fully differential signal path maximizes common mode rejection and eliminates the need to generate a negative voltage rail. Built-in IO amplifiers allow a bipolar analog input to be converted to mid-rail (VMR) referenced differential signal using only passive external components. Buffered and unbuffered analog outputs are provided as well as an additional differential amplifier and two programmable oscillator outputs.

Functions

- Filters (low pass, high pass, band pass, band stop, pole-zero)
  - Up to 8th order filter in a single chip
  - Butterworth, Chebyshev, Inverse Chebyshev, Elliptic, Bessel
  - Customizable gain/attenuation
  - Up to 400kHz
- Gain/attenuation stages with optional limiter and voltage control
- PID control loops: Multiplier, integrator, differentiator, sum / difference
- Signal linearization and compression (8-bit table lookup)
- Programmable oscillator (61.515 Hz – 16MHz)
- Differential amplifier and comparator
- Voltage reference
- Zero crossing detector
- See Available CAMs sections for complete list

Pinout

Pin	Signal	Description
1	PORB	Power on reset signal - active low, internal 10K pullup
2	INP	Differential input positive
3	INN	Differential input negative
4	RON	Rauch filter output negative
5	ROP	Rauch filter output positive
6	GND	Ground (0V reference)
7	VDD	Chip power supply 3.3V
8	BUFOUTN	Buffered sample & hold output negative
9	BUFOUTP	Buffered sample & hold output positive
10	OUTP	Unbuffered output positive. May also be configured for digital (e.g. comparator) output.
11	OUTN	Unbuffered output negative. May also be configured for digital (e.g. comparator) output.
12	AMPINP	Differential amplifier input positive
13	AMPINN	Differential amplifier input negative
14	VDD	Chip power supply 3.3V
15	GND	Ground (0V reference)
16	AMPOUTN	Differential amplifier output negative
17	AMPOUTP	Differential amplifier output positive
18	CLKOUTB	Digital output 2 (default inverted clock output)
19	CLKOUT	Digital output 1 (default clock output)
20	EXT_WB	External SPI interface write protect - active low, internal 10K pulldown. Pin must be driven high externally to program EEPROM.
21	EXT_CSB	External SPI interface chip select - active low
22	VMR	Mid-rail reference voltage ~1.5V
23	NC	No internal connection
24	NC	No internal connection
25	VDD	Chip power supply 3.3V
26	GND	Ground (0V reference)
27	NC	No internal connection
28	LCCb	Local configuration complete (done) - active low
29	EXT_MISO	External SPI interface serial data output from EEPROM
30	EXT_SCK	External SPI interface serial clock
31	EXT_SEL	External SPI interface select - enables external pin access to EEPROM when high. 10K internal pulldown. Pin must be driven high to program EEPROM.
32	EXT_MOSI	External SPI interface serial data input to EEPROM

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Power Supply	VDD	-0.5	-	3.6 V	V	Referenced to GND
Max power dissipation	Pmax	-	-	0.4	W	
Input Voltage	Vin	VSS-0.5	-	VDD+0.5	V	
Ambient Operating Temperature	Top	-40	-	85	°C	
Storage Temperature	Tstg	-40		125	°C	
Lead Temperature (soldering, 10 second)	Tsolder			260	°C	

Electrical Characteristics

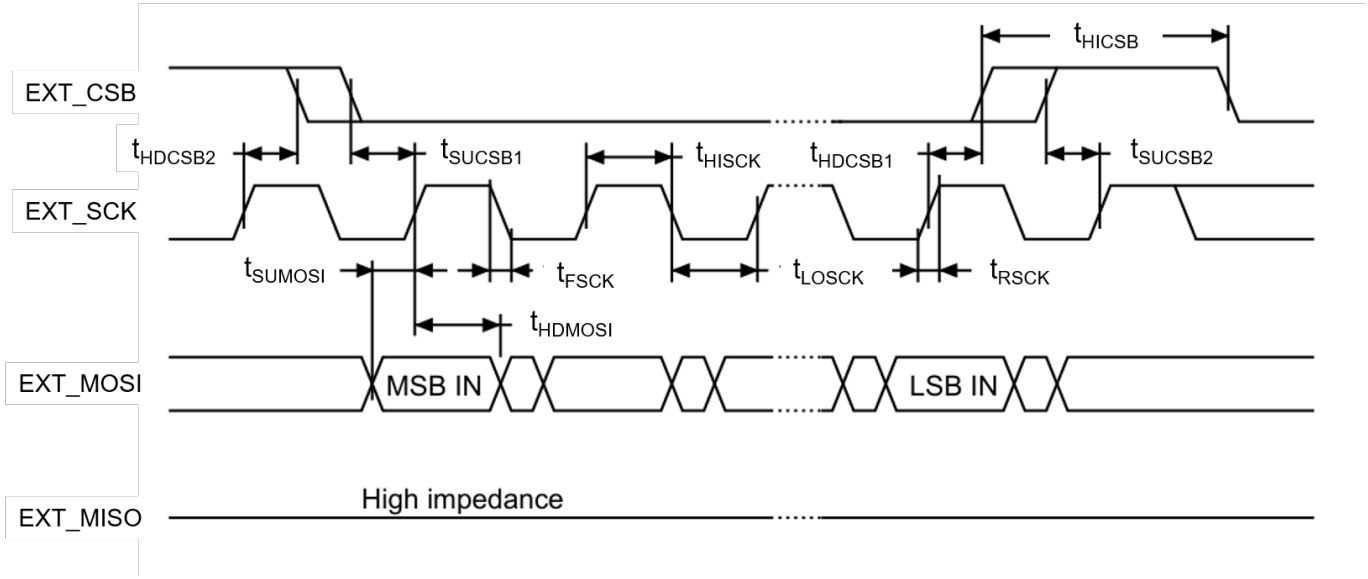
Parameter	Symbol	Units	Min	Typ	Max	Comment
Supply Voltage	VDD	V	3.0	3.3	3.6	
Supply Current	IDD	mA		56		Note 1
Power Dissipation	PD	mW		185		Note 1
Input Common Mode Voltage	VICM	V		1.5		
Output Common Mode Voltage	VOCM	V		1.5		
Input Voltage Range	VIN	Vinpp		2.75		VMR = 1.5V
Output Voltage Swing	VOUT	Voutpp		2.75		VMR = 1.5V
Output Load Resistance	RL	kΩ	1			
Output Load Capacitance	CL	pF			100	
Input Impedance INP, INN, AMPINP, AMPINN	RIN	MΩ	10			
Output Impedance ROUTP, ROUTN, AMPOUTP, AMPOUTN	ROUT	Ω		33		
Pull-up resistance PORB	RPU	Ω		10K		
Pull-down resistance EXT_WB, EXT_SEL	RPD	Ω		10K		
Reset Configuration Time	tRST	ms			100	Delay from PORB input signal rising to LCCb pin rising.

1. Configured as 8th order Butterworth LPF

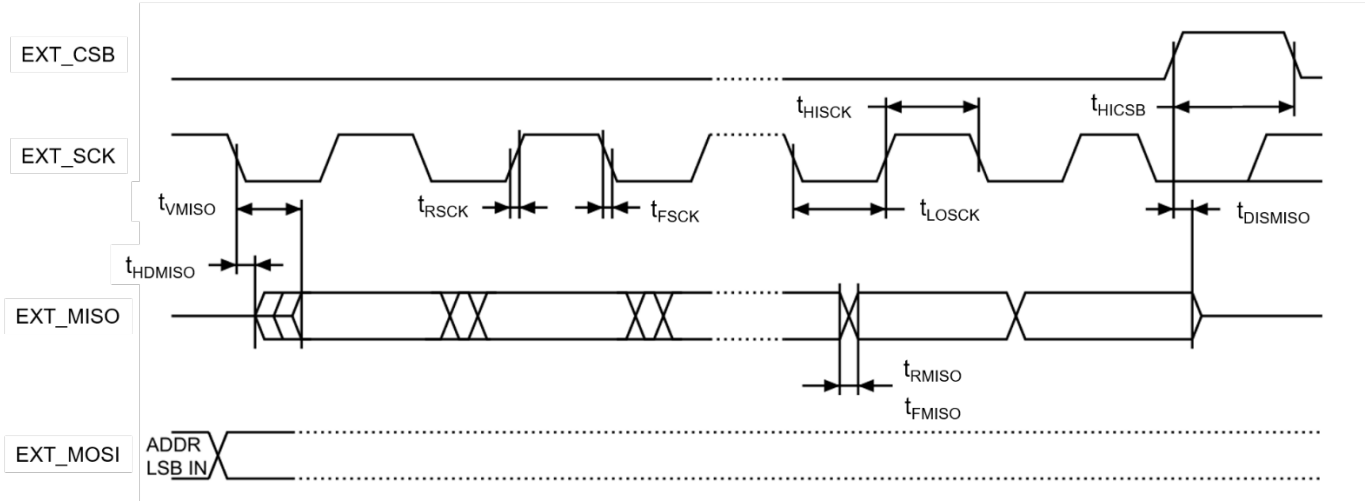
Programming Interface

When EXT_SEL is driven high, the remainder of the EXT pins are routed to the internal SPI EEPROM module (M95080-R). The EXT_WB pin must be driven high to enable writes to the EEPROM. Following programming of the EEPROM, the EXT_SEL pin must be returned low and the OTC9300L module must be power-cycled or the PORb pin toggled low for at least 1ms then high to force the AN231 to load the new configuration from the EEPROM. Refer to the timing diagrams below for definitions of each parameter in the timing table.

Serial Input Timing



Serial Output Timing



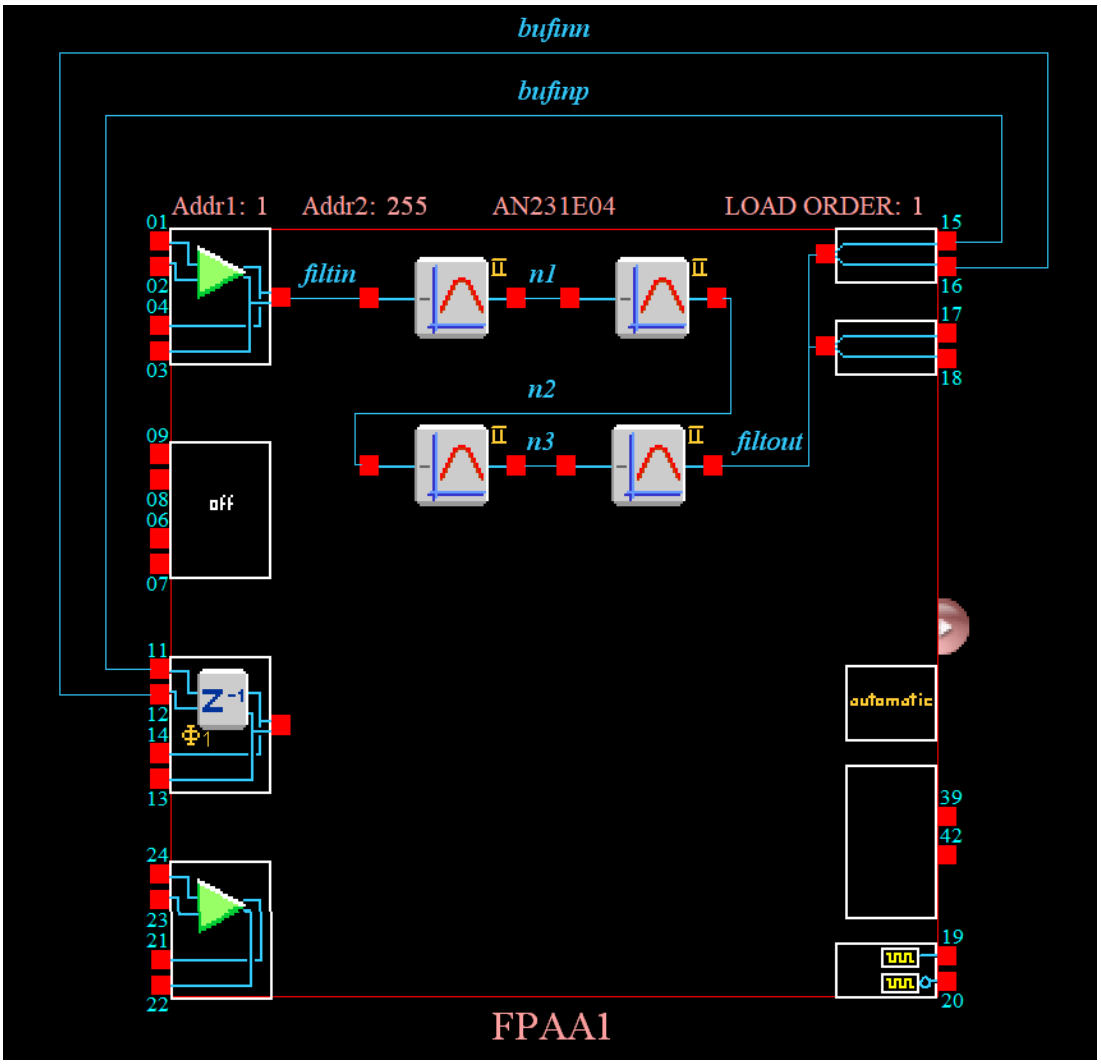
Symbol	Parameter	Min	Max	Unit
fSCK	EXT_SCK frequency	D.C.	10	MHz
tSUCSB1	EXT_CSB active setup time	30	-	Ns
tSUCSB2	EXT_CSB not active setup time	30	-	Ns
tHICSB	EXT_CSB deselect time	40	-	Ns
tHDCSB1	EXT_CSB active hold time	30	-	Ns
tHDCSB2	EXT_CSB not active hold time	30	-	Ns
tHISCK	EXT_SCK high time	40	-	Ns
tLOSCK	EXT_SCK low time	40	-	Ns
tRSCK	EXT_SCK rise time	-	2	Us
tFSCK	EXT_SCK fall time	-	2	Us
tSUMOSI	EXT_MOSI setup time	10	-	Ns
tHDMOSI	EXT_MOSI hold time	10	-	Ns
tDISMISO	EXT_MISO disable time	-	40	Ns
tVMISO	EXT_SCK low to EXT_MISO valid	-	40	Ns
tHDMISO	EXT_MISO hold time	0	-	Ns
tRMISO	EXT_MISO rise time	-	40	Ns
tFMISO	EXT_MISO fall time	-	40	Ns
tWRITE	Write time	-	5	Ms

FPAA Connections

Chameleon™ modules are configured using Okika's Anadigm Designer 2 software, which also provides accurate and fast simulation capability. The table below defines the connections between the module pins and FPAA pins. A wide variety of circuits can be implemented using any of the approved CAMs within the connection constraints described in this table.

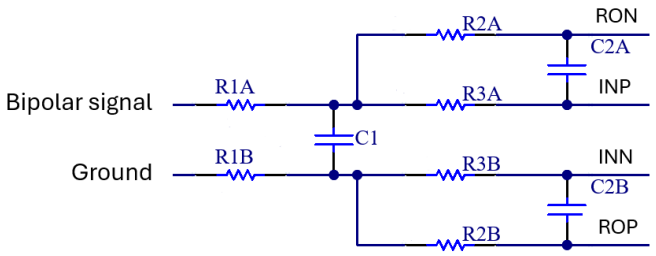
IOCell	FPAA Pins	FPAA Name	Chameleon™ Module Pins	Intended Use
1	1 2 3 4	I1P I1N O1N O1P	INP INN RON ROP	Analog Input
2	6 7 8 9	O2P O2N I2N I2P	Not used	None
3	11 12 13 14	I3P I3N O3N O3P	bufinp(internal) bufinn(internal) BUFOUTN BUFOUTP	Drive off chip circuitry such as analog to digital converter (ADC) from IOCell3 configured as Sample & Hold.
4	21 22 23 24	O4P O4N I4N I4P	AMPOUTP AMPOUTN AMPINN AMPINP	Independent differential amplifier for customer circuits such as a Rauch output smoothing filter. May also be used for secondary analog input.
5	15 16	IO5P IO5N	bufinp(internal) bufinn(internal)	Internal connection of signal to IOCell3 buffer.
6	17 18	IO6P IO6N	OUTP OUTN	Unbuffered analog output. May also be used for digital outputs.
7	19 20	IO7P IO7N	CLKOUT CLKOUTB	Clock outputs. May also be used for comparator outputs or additional unbuffered analog outputs.
Digital	39 42	LCC_B MEMCLK	LCCb Internal use	Reserved for LCCb (done) signal and internal MEMCLK.

Example FPAA connections are shown below in the example case of an 8th order bandpass filter. Hardwire connections in the module are made from pin 15 to pin 11 and from pin 16 to pin 12. These connections are labeled bufinp and bufinn and should be included in any custom configurations implemented in the OTC9300L.



Analog Input

The analog input of the module is expected to be a differential input to INP and INN with signals centered at VMR (1.5V). Many analog signal sources create bipolar signals referenced to ground. These bipolar inputs can be easily converted to the required levels using a Rauch filter formed by the input amplifier and passive components as shown below. This structure can also be used to interface to differential signals that have a different common mode voltage.



Gain

G = R2 / R1

Low Pass Filter Cutoff Frequency

Fo = [1 / (2*π*R2)] * SQRT[(R1+R2) / (2*C1*C2*R1)]

Filter Quality Factor

Q = SQRT[(C1*R1) / (2*C2*(R1+R2))]

To determine component values for required values of gain, corner frequency and Q, first select a suitable value for R1 (e.g. 10kΩ) and then use the following equations to calculate the other component values:

R2 = R1*G
R3 = R1*G / (G+1)
C1 = Q*(G+1) / (2*π*G*Fo*R1)
C2 = 1 / (4*π*G*Fo*Q*R1)

Suggested component values for different filter frequencies are listed below.

	20kHz	50kHz	100kHz	200kHz	500kHz	1 MHz
R1	10K	10K	10K	10K	4.7K	2.2K
R2	10K	10K	10K	10K	4.7K	2.2K
R3	4.7K	4.7K	4.7K	4.7K	2.2K	1.0K
C1	1nF	390pF	220pF	100pF	86pF	100pF
C2	470pF	220pF	100pF	47pF	47pF	47pF
F0	23,215	54,335	107,302	232,151	532,628	1,055,233
Q	0.729	0.666	0.742	0.729	0.676	0.729

Part Numbering

OTC9300L

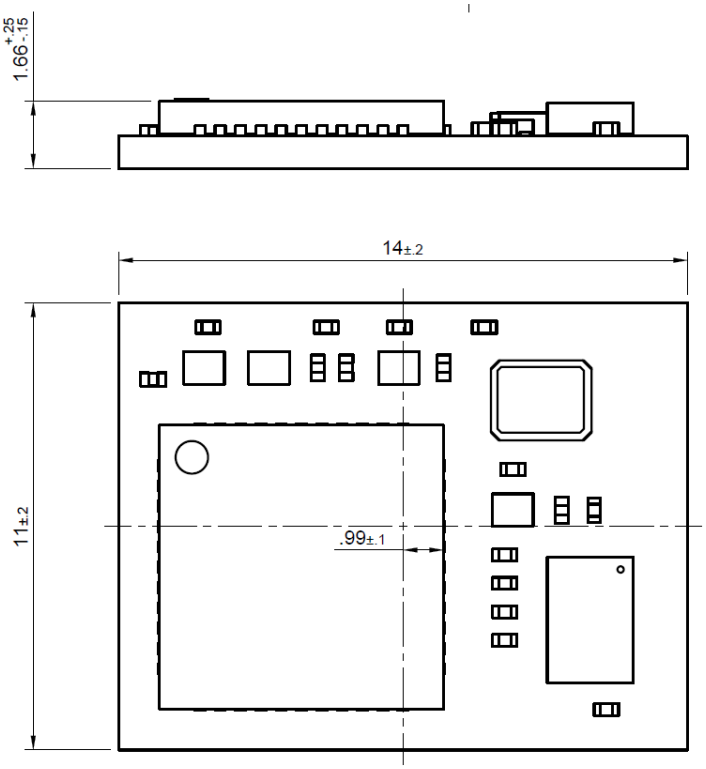
L = LGA32 form factor

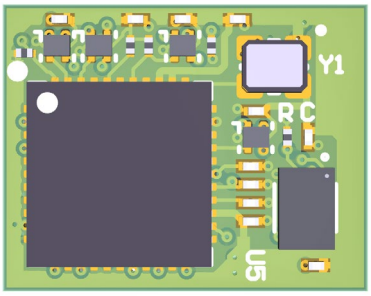
00 = Unprogrammed Chameleon™ module

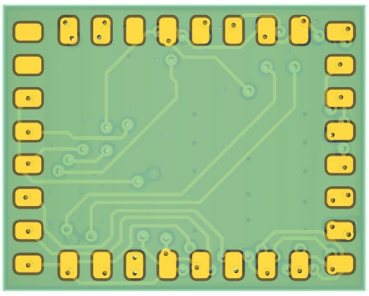
93 = AN231 EEPROM module

Okika Technologies Corporation

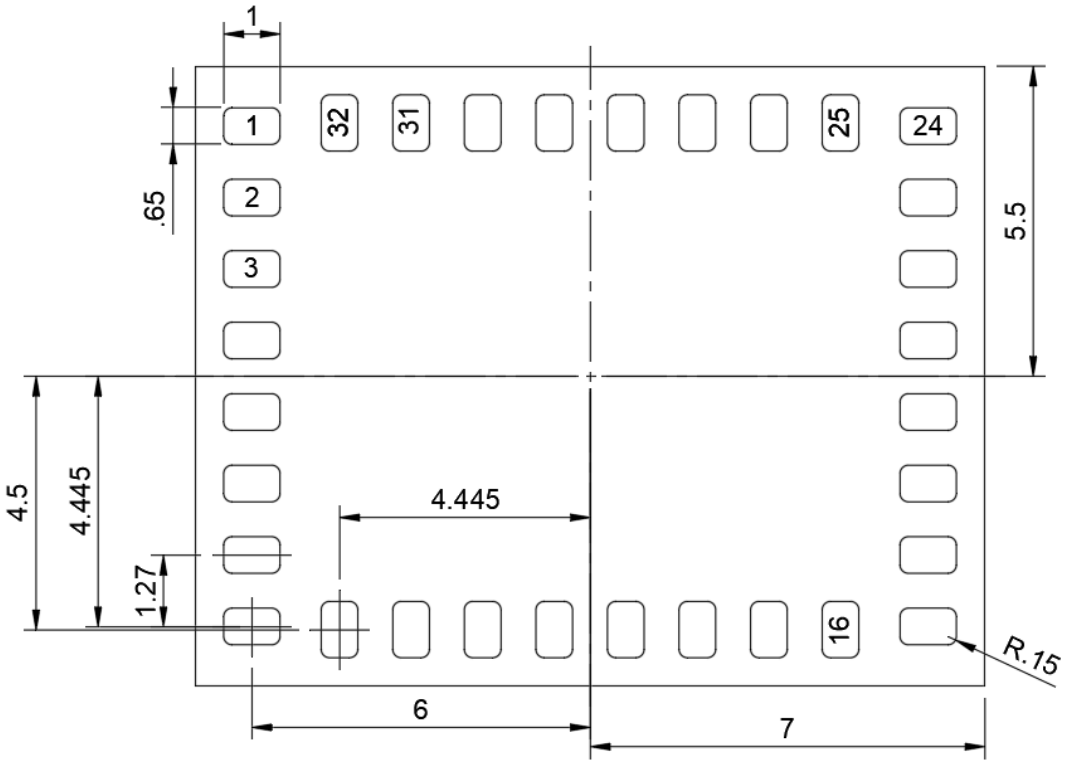
Mechanical Drawing







PCB Footprint (Top View)



Available CAMs

Name	Description
ADC-SAR	Analog to Digital Converter (SAR) 8-bit 250ksps
Comparator	Comparator
DelayLine	Programmable Delay
Differentiator	Inverting Differentiator
Divider	Divider
FilterBilinear	Bilinear Filter
FilterBiquad	Biquadratic Filter
FilterDCBlockLP	DC Blocking HPF with Optional LPF
FilterLowFreqBilinear	Low Corner Frequency Bilinear LPF (External Caps)
FilterVoltageControlled	Voltage Controlled Filter
GainHalf	Half Cycle Gain Stage
GainHold	Half Cycle Inverting Gain Stage with Hold
GainInv	Inverting Gain Stage
GainLimiter	Gain Stage with Output Voltage Limiting
GainPolarity	Gain Stage with Polarity Control
GainSwitch	Gain Stage with Switchable Inputs
GainVoltageControlled	Voltage Controlled Variable Gain Stage
Hold	Sample and Hold
HoldVoltageControlled	Voltage Controlled Sample and Hold
Integrator	Integrator
IntegratorHold	Window Integrator with Hold
Multiplier	Multiplier
MultiplierFilterLowFreq	Multiplier with Low Corner Frequency LPF (External Caps)
OscillatorSawSqr	Sawtooth and Square Wave Oscillator
OscillatorSine	Sinewave Oscillator
PeakDetect	Peak Detector
PeakDetect2	Peak Detector
PeakDetectExt	Peak Detector (External Caps)
PeriodicWave	Arbitrary Periodic Waveform Generator
RectifierFilter	Rectifier with Low Pass Filter
RectifierHalf	Half Cycle Rectifier
RectifierHold	Half Cycle Inverting Rectifier with Hold
SquareRoot	Square Root
SumBiquad	Sum/Difference Stage with Biquadratic Filter
SumDiff	Half Cycle Sum/Difference Stage
SumFilter	Sum/Difference Stage with Low Pass Filter
SumIntegrator	Sum/Difference Integrator
SumInv	Inverting Sum Stage
TransferFunction	User-defined Voltage Transfer Function
Transimpedance	Transimpedance Amplifier
Voltage	DC Voltage Source
ZeroCross	Zero Crossing Detector

Power Supply Decoupling

Power supply decoupling capacitors are included within the module. A single external 0.1uF decoupling capacitor between pins 6 and 7 of the module is sufficient. Additional capacitors between pins 14 and 15, and between pins 25 and 26 are optional.

Performance Metrics

Chameleon™ modules can be used over a wide range of frequencies. The practical limits depend on the CAM and the Unity Gain Bandwidth of the internal amplifiers. The tables below summarize performance metrics for select CAMs. Clock frequency limitations for the AN231 are included for each CAM with the Anadigm Designer 2 software. Most CAMs have a maximum recommended clock frequency of 4MHz on the AN231.

CAM	LPF slope (dB/octave)	Max Gain per instance	AN231 18 MHz UGB 4 MHz clock
FilterBilinear	5-6	20 (26dB)	400 kHz
FilterBiquad	9-12	20 (26dB)	400 kHz

CAM	Performance Metric	AN231 4 MHz clock
ADC-SAR	Sample Rate Max signal frequency	250 ksps 125 kHz
GainInv	Minimum Gain Maximum Gain	0.01 (-40dB) 100 (40dB)
PeriodicWave	Maximum sample clock	500 kHz

For further CAM performance details, refer to the AN231 data sheet.

Revision History

Date	Description
7/9/2026	Initial release