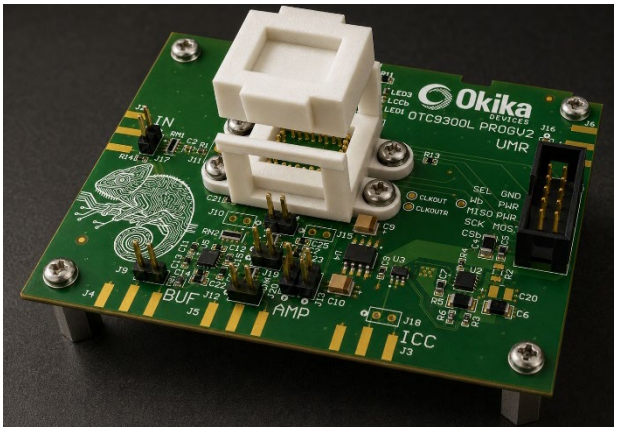
Summary

The Chameleon™ Programming Board (OTC9300L PROGV2) is a socketed test fixture for programming and testing the Chameleon family of OTC93xxL Field Programmable Analog Modules. A 10-pin keyed programming interface allows a standard 3.3 V SPI EEPROM programmer or external microcontroller to be used to load custom configurations into the EEPROM of blank Chameleon modules. Header pins and optional SMA connector pads facilitate interfacing the module IO pins for circuit evaluation, and onboard components are available for typical single-channel and dual-channel use cases.



Features

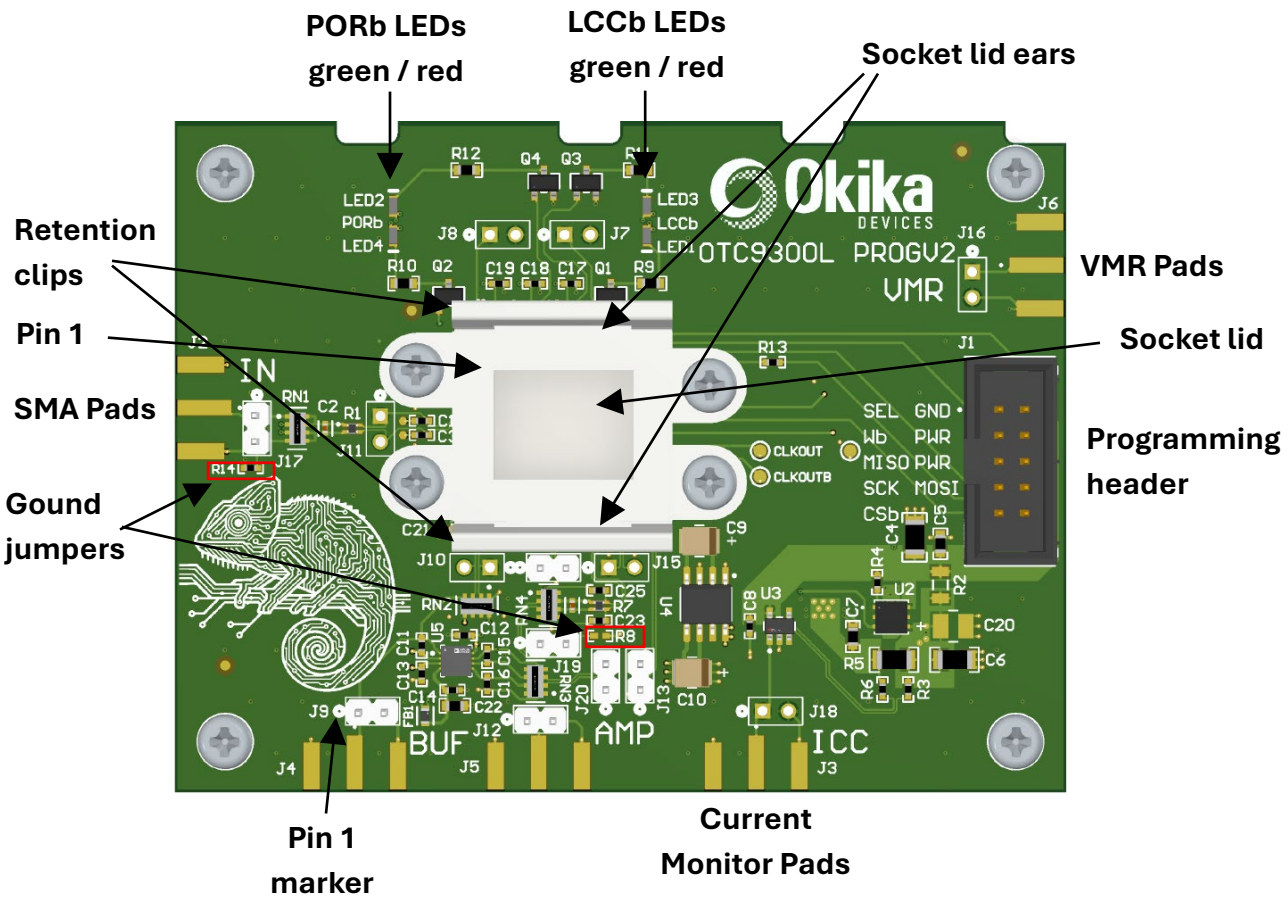
- Spring pin socket with keyed lid and retention clips
- Total Phase Cheetah compatible 10-pin header for SPI and GPIO (SEL, Wb)
- Optional second-order active low-pass Rauch filter on each analog input
- Differential-to-single-ended converter on each analog output
- Pads for optional SMA connectors
- 3.3 V regulator with optional bypass
- -3.3 V voltage inverter for ground-referenced single-ended output
- Regulator power-good output connected to module PORb.
- Current-sense resistor and amplifier for 3.3 V rail with 5 V/A output and SMA connector pads
- SMA connector and header pads for mid-rail reference (VMR) output
- LED and driver for LCCb (red when high, green when low)
- LED and driver for PORb (red when low, green when high)
- Optional through hole headers for differential probing, test points, and harnessing

Pin Staggering

The spring pin locations are staggered slightly to maximize the gap between each pin while still contacting the module pads. This staggering is normal.

Programming Header Pinout

Pin	Signal	Description
1	SEL	EEPROM interface select. Drive high to connect SPI pins from the programming header to the EEPROM in the module.
2	GND	Ground
3	Wb	Active low EEPROM write protect signal. Drive high to enable writes to the EEPROM.
4	PWR	Power supply. Shorted to pin 6. Apply regulated +5 V here to power both the programming board and installed module.
5	MISO	SPI data output from the module (input to programmer / microcontroller).
6	PWR	Power supply. Shorted to pin 4.
7	SCK	SPI clock signal.
8	MOSI	SPI data input to the module (output from programmer / microcontroller).
9	CSb	Active low EEPROM chip select.
10	GND	Ground



Input / Output Headers

Signal	Conn	Default P / NP[1]	Description
IN	J17	P	Primary single-ended analog input to Rauch. + on J17-1, -/GND on J17-2.
	J2	NP	
IN2	J19	P	Secondary single-ended analog input to Rauch. + on J19-1, -/GND on J19-2.
BUFSE	J9	P	Single-ended analog output converted from J10 differential signals tied to module pins 9 and 8 (O3 from FPAA). + on J9-1, GND on J9-2.
	J4	NP	
AMPSE	J12	P	Secondary single-ended analog output converted from J20 differential signal.
	J5	NP	
IN_P/N	J11	NP	Primary differential analog input to module pins 2 and 3 (I1 to FPAA). IN_P on J11-1, IN_N on J11-2.
AMPIN_P/N	J15	NP	Secondary differential analog input to module pins 12 and 13 (I4 to FPAA). AMPIN_P on J15-1, AMPIN_N on J15-2.
OUT	J14	P	Differential output from module pins 10 and 11 (IO6 from FPAA).
AMPOUT	J13	P	Differential output from module pins 17 and 16 (O4 from FPAA).
BUFOUT	J10	NP	Differential output from module pins 9 and 8 (O3 from FPAA).
SE2	J20	P	Differential signal input to converter for AMPSE single-ended output.
IMEAS	J18	NP	Current measurement output. I(A) = 0.2 * V(IMEAS). Output on J18-1, GND on J18-2.
	J3	NP	
VMR	J16	NP	Mid-rail voltage monitor. VMR on J16-1, GND on J16-2.
	J6	NP	
LCCb	J7	NP	Active low load configuration complete output monitor. LCCb on J7-1, GND on J7-2.
PORb	J8	NP	Active low power-on reset monitor / force. PORb on J8-1, GND on J8-2.

1. P = Populated, NP = Not Populated

The SMA edge connector pads are not populated (NP) by default. The footprint is compatible with TE Connectivity part number CONSMA020.062-G. NP 2-pin 0.1” pitch through-hole pads are compatible with Amphenol part number G800W306018EU or any similar header.

Electrical Characteristics

Parameter	Symbol	Units	Min	Typ	Max	Comment
Operating Temperature	TOP	°C	0		50	
Supply Voltage	VPWR	V	4.5	5.0	5.5	
Supply Current	IDD	mA		92		Note 1
SPI Interface IO Voltage	VIO	V		3.3		
SPI Input High Voltage	VIH	%VIO	80			
SPI Input Low Voltage	VIL	%VIO			20	
SPI Output High Voltage	VOH	%VIO	85			Current < 1mA
SPI Output Low Voltage	VOL	%VIO			15	Current < 1mA
SPI Clock Frequency	fSCK	MHz			10	Limited by EEPROM on module
Rauch filter nominal corner frequency	fRCIN	kHz		2300		Set by nominal resistor and capacitor values
Differential-to-single-ended output filter corner frequency	fRCOUT	kHz		3300		Set by nominal resistor and capacitor values
Rauch input filter gain	ARIN	V/V		1		
Output filter gain	AROUT	V/V		1		

1. Configured as 8th order Butterworth LPF

Input / Output Filters

Lowpass filters are provided at the inputs and outputs to serve as antialiasing filters and reconstruction filters. Resistors and capacitors work in conjunction with the IO amplifiers on the FPAA to implement the input filters. This also provides a convenient way to convert from ground-referenced input signals to VMR-centered differential signals used by the FPAA.

The default component values provide a gain of 1 set corner frequencies above the typical bandwidth of FPAA circuits such that they will be transparent in most use cases. Different gain and corner frequencies are possible by adjusting the component values. Resistor arrays (Bourns CAT16-F4 family) are used to improve resistor matching, shrink the circuitry and reduce the number of placed components. Footprint compatible thin-film arrays, such as the Susumu RM3216F family, can be used if lower 1/f noise is required or if gain is required by making the outer and inner resistors different values. It is also possible to solder 0402 discrete values across the array resistor pads to implement alternate Rauch filter circuits using the available array pads.

Ground Jumpers

The negative input of the IN (J2, J17) and IN2 (J19) connectors can be optionally tied to ground near the connector through R14 (IN) or R8 (IN2). For ground-referenced inputs, this provides a convenient place to tie the ground connection. By default R14 is installed, and J17-2 is shorted to ground. R8 is not installed by default.

Single / Dual IO

Chameleon modules may have single or dual IO. The programming board is designed to support both through a combination of population options and local wire jumpers. The table below describes typical connections for Single and Dual IO.

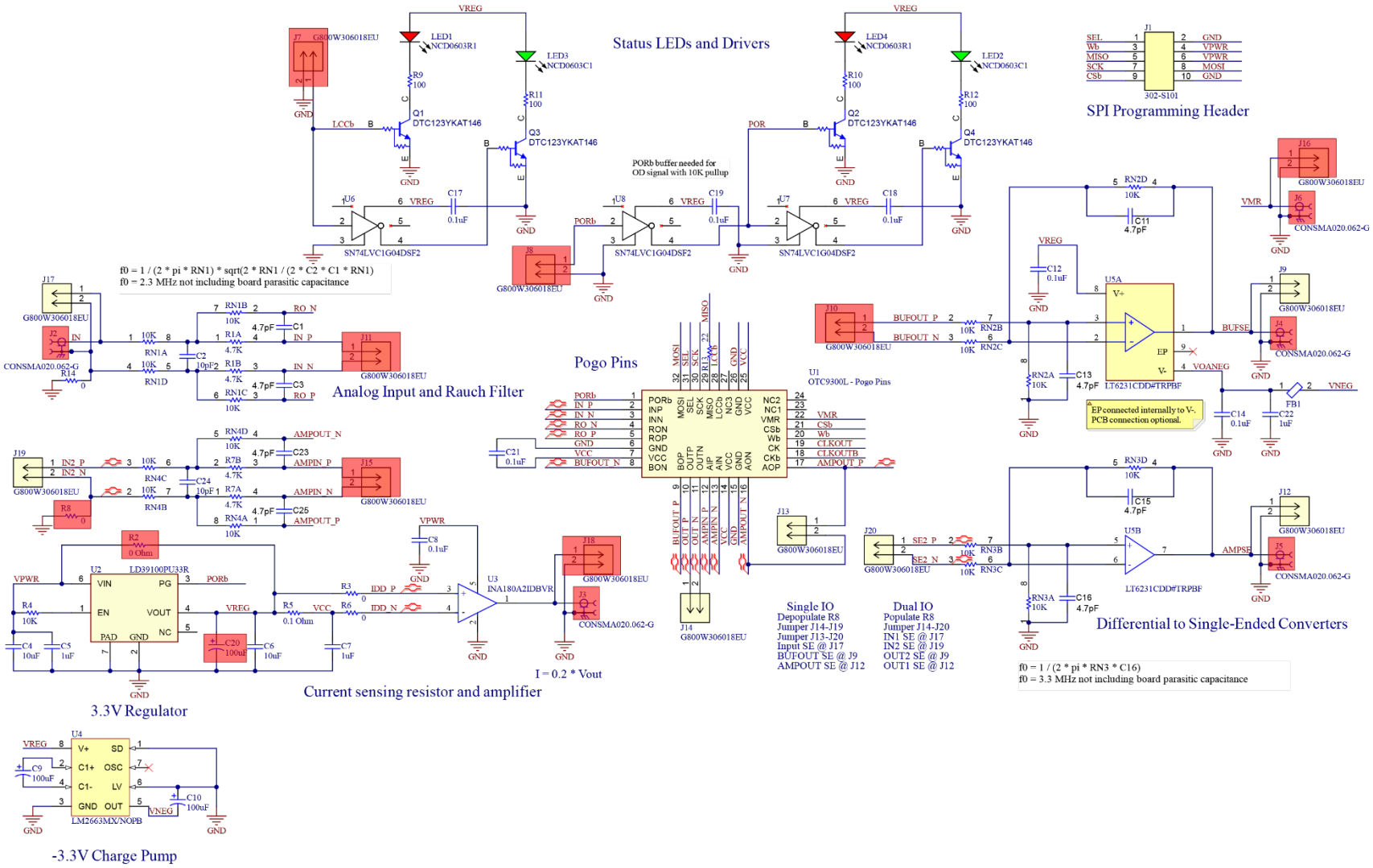
Single IO	**Dual IO**
Depopulate R8 and use AMP inputs for additional filtering	Populate R8 to enable input level shifting from ground-referenced to VMR-centered
Connect J14-1 to J19-1 and J14-2 to J19-2	Connect J14-1 to J20-1 and J14-2 to J20-2
Connect J13-1 to J20-1 and J13-2 to J20-2	Connect ground-referenced IN1 to J17
Connect ground-referenced input to J17	Connect ground-referenced IN2 to J19
Monitor ground-referenced output at J9	Monitor ground-referenced OUT2 at J9
Monitor ground-referenced AMPOUT at J12	Monitor ground-referenced OUT1 at J12

Socket and Lid Usage

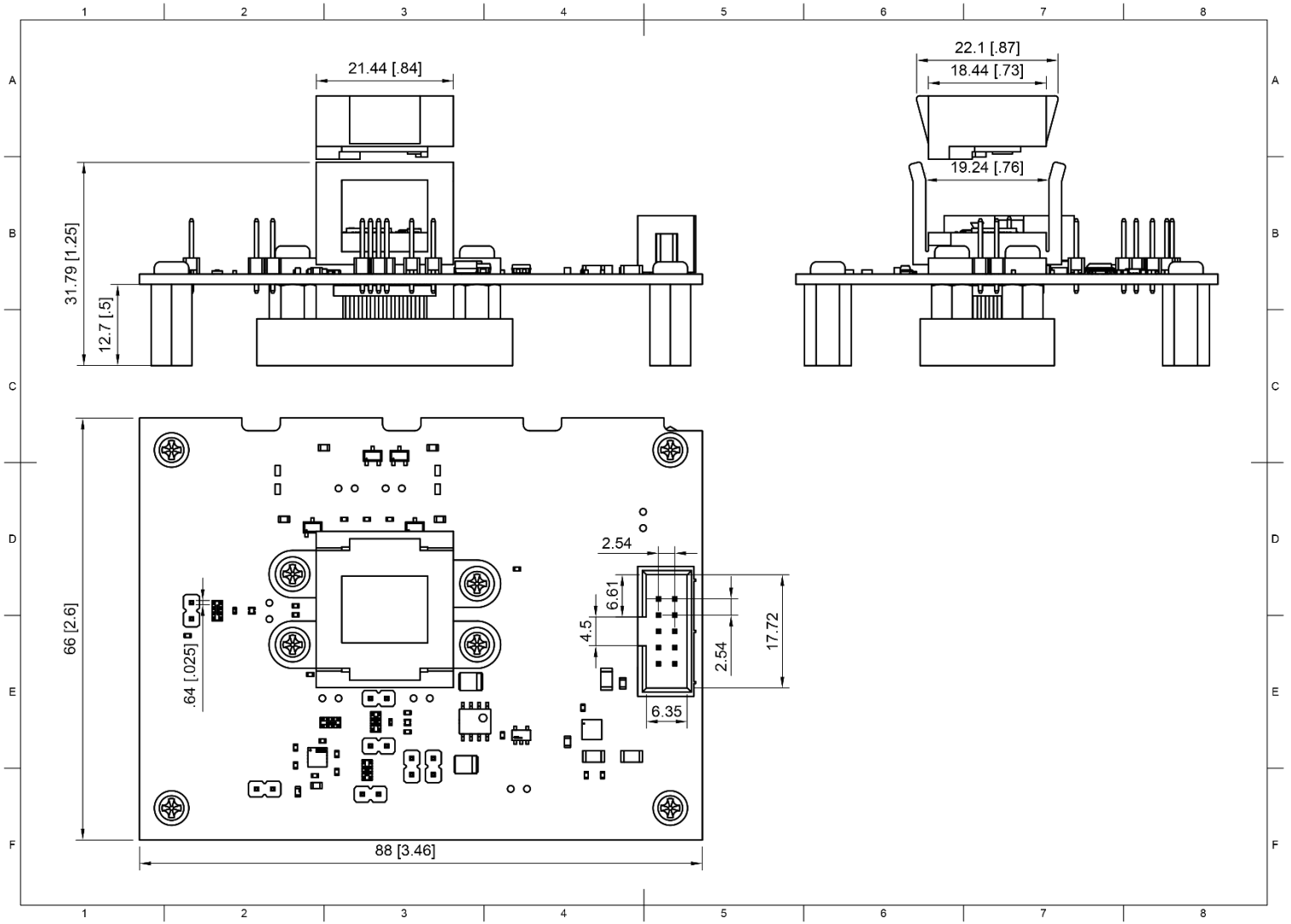
Carefully place a module within the socket body with the pin 1 mark in the upper left (keyed) corner of the socket. A vacuum pin may be helpful for module placement and removal. The spring pins are slightly below the top of the socket base, so module movement should be constrained on all sides when it is properly placed. Position the socket lid with the key in the upper left corner and the ears of the lid aligned with the openings in the retention clips. Push the lid down until the lid bottoms out against the socket body. In the process, the lid ears will push the retention clips out of the way until the ears clear the retention clips and the clips will snap back into place. Once the retention clips are above the lid ears, slowly release the lid and allow the spring force of the socket to hold the lid against the bottom of the retention clips. There will be a slight gap between the lid and the socket body during normal use.

To remove a module, ensure the board is powered down (no LEDs on) and push down on the lid and spread the retention clips apart to clear the lid ears while slowly releasing the lid. Once the ears are clear of the clips, pull the lid completely away from the retention clips and remove the module from the socket. Again, a vacuum pen may be useful.

Schematic


Status LEDs and Drivers
SPI Programming Header
Analog Input and Rauch Filter
Pogo Pins
Current sensing resistor and amplifier
3.3V Regulator
-3.3V Charge Pump
Differential to Single-Ended Converters
Single IO
Depopulate R8
Jumper J14-J19
Jumper J13-J20
Input SE @ J17
BUFOUT SE @ J9
AMPOUT SE @ J12
Dual IO
Populate R8
Jumper J14-J20
IN1 SE @ J17
IN2 SE @ J19
OUT2 SE @ J9
OUT1 SE @ J12
I = 0.2 * Vout
PORb buffer needed for OD signal with 10K pullup
f0 = 1 / (2 * pi * RN1) * sqrt(2 * RN1 / (2 * C2 * C1 * RN1))
f0 = 2.3 MHz not including board parasitic capacitance
f0 = 1 / (2 * pi * RN3 * C16)
f0 = 3.3 MHz not including board parasitic capacitance
EP connected internally to V-. PCB connection optional.

Mechanical Drawing



Revision History

Date	Description
7/20/2026	Initial release